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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Daniel R. Loughmiller et al.

Title: CIRCUIT AND METHOD FOR MEASURING AND FORCING AN INTERNAL VOLTAGE OF AN INTEGRATED CIRCUIT

Attorney Docket No.: 303.145US3

PATENT APPLICATION TRANSMITTAL

BOX PATENT APPLICATION
Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items and information (as indicated with an "X"):

X Return postcard.
X **CONTINUATION** of prior Patent Application No. 09/031,934 (under 37 CFR § 1.53(b)) comprising:
  X Specification (14 pgs, including claims numbered 1 through 18 and a 1 page Abstract).
  X Formal Drawing(s) (5 sheets).
  X Copy of signed Declaration and Power of Attorney (4 pgs) from prior application.
  X Incorporation by Reference: *The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied herewith, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.*
  X Check in the amount of $690.00 to pay the filing fee.
X Prior application is assigned of record to Micron Technology, Inc..
X Information Disclosure Statement (1 pgs), Form 1449 (1 pgs). References NOT enclosed, cited in prior application.
X Preliminary Amendment (1 pgs).

The filing fee has been calculated below as follows:

	No. Filed	No. Extra	Rate	Fee
TOTAL CLAIMS	1 - 20 =	0	x 18 =	**$0.00**
INDEPENDENT CLAIMS	1 - 3 =	0	x 78 =	**$0.00**
[ ] MULTIPLE DEPENDENT CLAIMS PRESENTED				**$0.00**
BASIC FEE				**$690.00**
TOTAL				**$690.00**

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S/N Unknown **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Daniel R. Loughmiller et al.	Examiner: Unknown
Serial No.:	Unknown	Group Art Unit: Unknown
Filed:	Herewith	Docket: 303.145US3
Title:	CIRCUIT AND METHOD FOR MEASURING AND FORCING AN INTERNAL VOLTAGE OF AN INTEGRATED CIRCUIT	

PRELIMINARY AMENDMENT

BOX PATENT APPLICATION
Commissioner for Patents
Washington, D.C. 20231

Please amend the above-identified patent application as follows:

IN THE SPECIFICATION

Please insert before the first sentence "This application is a continuation of U.S. Patent Application Serial No. 09/031,934, filed on February 27, 1998 (the '934 Application). The '934 Application is incorporated herein by reference."

IN THE CLAIMS

Please cancel claims 2-18 without prejudice.

Respectfully submitted,

DANIEL R. LOUGHMILLER ET AL.

By their Representatives,

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Printed Name Shawn Hise

Signature

CIRCUIT AND METHOD FOR MEASURING AND FORCING AN INTERNAL VOLTAGE OF AN INTEGRATED CIRCUIT

Technical Field of the Invention

The present invention relates generally to electronic circuits and in particular the present invention relates to a circuit and method for measuring and forcing an internal voltage of an integrated circuit.

Background of the Invention

Integrated circuits comprise a collection of transistors and other semiconductor devices interconnected on a semiconductor substrate. During production, an integrated circuit is encapsulated, for example, in a plastic body. Further, a passivation layer comprising silicon dioxide, for example, may be formed on the integrated circuit prior to encapsulation to protect the junctions and surfaces of the semiconductor devices of the integrated circuit from harmful environments. The integrated circuit interfaces with other components of a system via a number of metal pins that extend from the plastic body. The pins provide electrical connection to various internal points or nodes in the integrated circuit. Typically, many internal nodes in the circuit that can impact the performance of the integrated circuit are not connected to a pin.

For example, the substrate voltage is a measurable quantity that can affect the operation of an integrated circuit such as a refresh operation in a dynamic random access memory. However, the substrate voltage is not typically provided at a pin of the integrated circuit. If a problem is suspected with the substrate voltage once the integrated circuit is packaged or passivated, an engineer must remove at least a portion of the plastic casing or passivation layer or both and place a probe at the proper node to determine the voltage. Based on the measurement, process parameters may be adjusted for further production. However, this procedure is time consuming and subject to the accuracy of the set up of the testing equipment.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a circuit and method for measuring and forcing an internal voltage in an integrated circuit without having to remove either the plastic body or the passivation layer.

Summary of the Invention

The above mentioned problems with measuring internal voltages in an integrated circuit and other problems are addressed by the present invention and which will be understood by reading and studying the following specification. A circuit is described which measures voltages at internal nodes of an integrated circuit without removing a plastic body or a passivation layer.

In particular, the present invention describes a circuit for reading a voltage at a node of an integrated circuit. The circuit comprises a pass circuit that has an input coupled to the node of the integrated circuit. The circuit provides a measurement of the voltage at the node as an output to a pin. A reset circuit is coupled to the pass circuit and is operable to activate and reset the pass circuit. Finally, a pass control circuit is coupled to provide an output signal to the pass circuit that drives the pass circuit when active to pass the voltage at the node to the pin. The circuit can also force the voltage at the node of the integrated circuit by applying a voltage to the pin.

Brief Description of the Drawings

Figure 1 is a block diagram of an embodiment of the present invention;

Figure 2 is a schematic diagram of an embodiment of a read circuit for use in the block diagram of Figure 1;

Figures 3A through 3F are timing diagrams illustrating the operation of the embodiment of Figure 2;

Figure 4 is a schematic diagram of another embodiment of a read circuit for use with the block diagram of Figure 1; and

Figure 5A through 5J are timing diagrams illustrating the operation of the embodiment of Figure 4.

Detailed Description of the Invention

In the following detailed description of the illustrative embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific illustrative embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense.

Figure 1 is a block diagram of an illustrative embodiment of the present invention. Read circuit 10 is formed as a part of integrated circuit 12 on the same substrate with voltage source 14 and functional circuit 18. Although voltage source 14, read circuit 10 and functional circuit 18 are shown in separate locations of integrated circuit 12 in the embodiment of Figure 1, in other embodiments, components of read circuit 10 and voltage source 14 are intermingled with components of functional circuit 18 to conserve surface area on the substrate of integrated circuit 12 using techniques that are well known in the art. Voltage source 14 is coupled to functional circuit 18 and to read circuit 10. Functional circuit 18 is coupled to input/output pins 16 and 20. Further, read circuit 10 is also coupled to input/output pin 16. Functional circuit 18 may comprise, for example, a microprocessor, a memory device such as a dynamic random access memory, or a static random access memory or other typical integrated circuit. In other embodiments, integrated circuit 12 may also include more than one read circuit coupled to other voltage sources.

In operation, read circuit 10 is operable to provide two functions. First, read circuit 10 can measure a voltage output by voltage source 14 and pass this voltage to input/output pin 16. This is referred to as "read mode." Alternatively, read circuit 10 can receive a voltage at input/output pin 16 and force the voltage of voltage source 14 to a desired level. This is referred to as "force mode." Read circuit 10

also may be isolated from input/output pin 16 so as to allow functional circuit 18 to use input/output pin 16. The circuits of Figures 2 and 4 illustrate embodiments of read circuit 10 and the read mode of each is described below. The circuits are not limited to just reading a voltage. The circuits also operate in a "force mode." A person of ordinary skill in the art will understand that the circuits enter force mode by providing an input voltage at the pin of integrated circuit 12 and then operating the circuit in the same manner as described for read mode.

Figure 2 is a block diagram of a read circuit, indicated generally at 110, that reads a voltage in integrated circuit 12. Advantageously, circuit 110 measures and forces negative voltages such as a substrate voltage, V_{bb}, at node 114 using pin 116. In further embodiments node 114 is coupled to other appropriate points or nodes in integrated circuit 12 which are not normally coupled directly to an input/output pin 20 of integrated circuit 12.

Circuit 110 comprises three main components delineated by broken lines surrounding electrical circuitry: pass circuit 118, pass control circuit 120 and reset circuit 122. Pass circuit 118 comprises n-channel MOS transistor 124 that is coupled to pass the voltage at node 114 to output pin 116 in response to signals from reset circuit 122 and pass control circuit 120. A gate of transistor 124 is coupled to receive a control signal from pass control circuit 120. A source of transistor 124 is coupled to output pin 116 and a drain of transistor 124 is coupled to node 126.

Reset circuit 122 comprises n-channel MOS transistor 128 and p-channel MOS transistor 130 that are coupled to prevent pass circuit 118 from passing a voltage to pin 116 in response to signals from pass control circuit 120. Transistor 128 includes a source that is coupled to ground potential. Further, a gate of transistor 128 is coupled to node 132. A drain of transistor 130 is coupled to a drain of transistor 128. A source of transistor 130 is coupled to node 126 and a gate of transistor 130 is coupled to node 134. Finally, a substrate of transistor 130 is coupled to power supply voltage, V_{CC}.

Pass control circuit 120 produces control signals to activate read circuit 118 to pass a voltage to output pin 116. Pass control circuit 120 comprises first and second

n-channel MOS transistors 136 and 138, p-channel transistor 140, and inverter 142. Inverter 142 is coupled between an input signal, labelled READ, from a test signal generator on integrated circuit 12 and node 132. The READ signal is also provided to read circuit 118 at the gate of transistor 124. A gate of transistor 140 and a gate of transistor 138 are coupled to node 132. A source and substrate of transistor 140 are coupled to the supply voltage, V_{CC}. A drain of transistor 140, a drain of transistor 138 and a gate of transistor 136 are coupled together at node 134. A source of transistor 136 is coupled to node 126. Finally, a source of transistor 138 is coupled to a drain of transistor 136 at node 114. Node 114 also receives the voltage to be read by circuit 110.

In operation, circuit 110 passes the voltage at node 114 to output pin 116. Figures 3A through 3F are timing diagrams that show voltage levels of identified nodes in circuit 110 as a function of time. At time t_1, the READ signal is brought to a high logic level such as 5 volts, for example. In response, transistor 124 turns "on". Further, inverter 142 forces node 132 to ground potential thus turning "off" transistors 128 and 138 and turning on transistor 140. It is noted that a transistor is "on" if a voltage is applied to the gate that creates a conduction channel between source and drain of the transistor. Otherwise, the transistor is said to be "off." With transistor 140 on, node 134 reaches the supply voltage, V_{CC}, which turns on transistor 136. Thus, the voltage at node 114 is passed to node 126 by transistor 136 and from node 126 to output pin 116 by transistor 124. It is noted that the voltage at node 134 also turns off transistor 130 and assures that there will be no leakage path through transistors 128 and 130.

Circuit 110 also allows pass circuit 118 to be deactivated and isolated from pin 116. At time t_2, the READ signal is brought to a low logic level of approximately zero volts thus turning off pass gate 124. Inverter 142 forces node 132 to a high logic level which turns off transistor 140 and turns on transistors 128 and 138. Further, transistor 138 forces node 134 to the level of the voltage at node 114, e.g. v_{bb}, which may be on the order of -1 volts. The negative voltage at node 134 further turns on transistor 130 and turns off transistor 136. Since transistor 136

is off, transistors 128 and 130 can pull node 126 to ground without fighting transistor 136 thus isolating circuit 110 from output pin 116.

Figure 4 is a block diagram of a read circuit, indicated generally at 210, that reads a voltage in integrated circuit 12 at node 214. Advantageously, circuit 210 reads a high positive voltage such as, for example, the voltage V_{CCP}. Circuit 210 comprises three main components: pass circuit 218, pass control circuit 220 and reset circuit 222. Pass circuit 218 comprises n-channel transistor 224 coupled to pass a voltage from node 214 to output pin 216. A gate of transistor 224 is coupled to node 226 through which transistor 224 receives control signals from reset circuit 222. Capacitor-coupled transistor 228 is coupled between node 226 and node 230.

Pass control circuit 220 comprises a ring oscillator or other appropriate circuit for creating an oscillating output signal at node 230. For example, pass control circuit 220 comprises inverter 232, NOR-gate 234, and inverters 236a through 236d. Inverter 132 is coupled to a first input of NOR-gate 234 at node 233. Inverters 236a through 236d are coupled in series to an output of NOR-gate 234. An output of inverter 236d is coupled to a second input of NOR-gate 234. The number of inverters used in pass control circuit 220 can be varied as necessary for an application so long as the output of pass control circuit 220 provides an oscillating signal at node 230. Pass control circuit 220 receives a READ signal at an input to inverter 232 to initiate the oscillating output of pass control circuit 220.

Reset circuit 222 is operable to prevent pass circuit 218 from passing a voltage to output pin 216. Reset circuit 222 comprises NAND-gate 238 that receives the inverted READ signal of node 233 at one input and a RESET signal at a second input. The READ and RESET signals are produced by a test signal generator on integrated circuit 12. The output of NAND-gate 238 is coupled to inverter 240. Inverter 240 is coupled to a gate of transistor 242 at node 244. Inverter 246 receives the READ signal at its input and is coupled at the output to a drain of transistor 242 at node 248. A source of transistor 242 is coupled to pass circuit 218 at node 226. A drain of a second transistor 250 is coupled to node 226. A source of transistor 250 is coupled to ground potential. NOR-gate 252 is coupled at its output to a gate

of transistor 250 at node 254. The RESET signal is coupled to a first input to NOR-gate 252. A second input to NOR-gate 252 receives the READ signal.

In operation, circuit 210 is operable to read a voltage at node 214 and provide the output at output pin 216. The operation of circuit 210 can be divided into three parts based on the values of the READ and RESET signals.

At time t_1 in Figures 5A through 5J, the READ signal is set to a low logic level of approximately ground potential and the RESET signal is set to a high logic level of, for example, 5 volts. Inverter 232 sets node 233 at a high logic level such that the output of pass control circuit 220 at node 230 is maintained at a low logic level. In this state, NOR-gate 252 outputs a low logic level at node 254 and thus transistor 250 is turned off. Further, transistor 242 is turned on by a high logic value at node 244 and a high logic value at node 248. Thus, node 226 is precharged to the supply voltage, V_{CC}, less the threshold voltage, V_T.

At time t_2, the voltage at node 214 can be read by bringing the READ signal to a high logic level while maintaining the RESET signal at a high logic level. At this time, node 244 is reduced to a low logic level and transistor 242 is turned off isolating reset circuit 222 from pass circuit 218. Inverter 232 produces a low logic level at node 233 which starts the output of pass control circuit 220 at node 230 to oscillate. As is well known in the art, the charge on a capacitor cannot change instantaneously, so node 226 follows the oscillation of node 230. The peak voltage on node 226 is higher than V_{CCP} by at least one V_T, thus the full value of V_{CCP} is passed to pin 216 by transistor 224.

At time t_3, pin 216 is isolated from circuit 210. The READ and RESET signals are both taken to ground potential. Node 233 returns to a high logic level and the output of pass control circuit 220 ceases to oscillate at node 230. Further, node 244 stays at ground potential and transistor 242 stays off. Node 254 goes to a high logic level turning on transistor 250 and bringing node 226 to a low logic level so as to turn off transistor 224 and isolate circuit 210 from pin 216. Once isolated, node 116 is allowed to float and decays over time as shown in Figure 5J.

Conclusion

By incorporating circuit 110, circuit 210 or both onto the same substrate as integrated circuit 12, it is possible to accurately measure or force internal voltages of an integrated circuit without the time consuming process of removing the packaging or passivation layer or both. Thus, engineers can easily monitor the output of a fabrication line and make adjustments as necessary to assure that specifications for the internal voltages are being met. For example, in production of dynamic random access memory (DRAM) device, engineers can monitor both V_{bb} and V_{CCP} to assure compliance with specifications. During a production run, a number of DRAMs are fabricated that include either circuit 110, circuit 210 or an equivalent. The engineer selects at least one of the DRAMs to test the voltage at the node such as V_{bb} or V_{CCP} or both. If the values are not acceptable, the engineer can adjust process parameters to correct the error so that future integrated circuits produced on the line will function properly.

Further, engineers can use circuit 110 or 210 to determine an a acceptable operating voltage for the internal node. First, an integrated circuit is fabricated that includes a functional circuit and the read circuit. The engineer selects a voltage for the internal node and applies the voltage to the pin. The read circuit forces this voltage on the node of the integrated circuit. The engineer can then test the functional circuit to assess its operation with the forced voltage on the node. Based on the tests, the engineer can adjust the voltage forced on the node until the functional circuit operates acceptably.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. For example, other circuits that produce an oscillating output may be substituted for the ring oscillator shown in Figure 3. Further, the type of integrated circuit 12 and the voltage being measured with circuit

110 and 210 may be varied without departing from the spirit and scope of the present invention.

What is claimed is:

1. A circuit for reading a voltage at a node of an integrated circuit, the circuit comprising:

a pass circuit coupled between the node of the integrated circuit and a pin of the integrated circuit;

a reset circuit coupled to the pass circuit and operable to activate and reset the pass circuit; and

a pass control circuit coupled to the pass circuit that provides an output signal to selectively drive the pass circuit to pass a voltage from the node to the pin of the integrated circuit.

2. The circuit of claim 1, wherein the pass circuit comprises a pass gate coupled between the node of the integrated circuit and the pin and controlled by signals from the pass control circuit and the reset circuit.

3. The circuit of claim 1, wherein the pass circuit comprises:

a pass gate having first, second and third terminals, the first terminal coupled to the control circuit, the second terminal coupled to the node of the integrated circuit, and the third terminal coupled to the pin; and

a capacitor coupled between the first terminal of the pass gate and the pass control circuit such that the control signal from the pass control circuit drives the voltage at the first terminal of the pass gate to cause a voltage at the second terminal to be passed to the third terminal so as to read the voltage at the node of the integrated circuit.

4. The circuit of claim 3, wherein the pass gate comprises an n-channel MOS transistor.

5. The circuit of claim 1, wherein the pass control circuit comprises a ring oscillator that is operable to provide an oscillating control signal to the pass circuit.

6. The circuit of claim 5, wherein the ring oscillator comprises:

a NOR gate coupled to receive a control signal at a first input;

a plurality of inverters coupled in series from an output of the NOR gate; and

an output of the inverter is coupled to a second input of the NOR gate so as to produce the oscillating output.

7. The circuit of claim 1, wherein the reset circuit comprises a pair of transistors coupled so as to generate a control voltage for the pass circuit that controls the ability of the pass circuit to pass the voltage at the node of the integrated circuit to the pin.

8. The circuit of claim 1, wherein the pass circuit comprises an n-channel MOS transistor coupled to pass a voltage from the pass control circuit to the pin.

9. The circuit of claim 1, wherein the pass control circuit comprises an n-channel MOS transistor having a drain coupled to the node of the integrated circuit and that is operable to be turned on to pass the voltage to the source of the transistor and to the pass circuit.

10. The circuit of claim 1, wherein the reset circuit comprises an n-channel transistor having a drain coupled to a drain of a p-channel transistor so as to provide a voltage at the source of the p-channel transistor to the pass circuit to prevent the pass circuit from passing a voltage to the output pin.

11. The circuit of claim 1, and wherein the pass control circuit comprises a pass coupled between the node of the integrated circuit and the pin such that the pass gate passes a voltage from the node to the pin in read mode and passes a voltage from the

pin to the node in a force mode so as to force the voltage at the node to a selected value.

12. An integrated circuit, comprising:

a plurality of semiconductor devices formed on a semiconductor substrate coupled together to perform a function having input and output pins and including at least one internal node having a measurable voltage; and

at least one circuit, coupled to the internal node, that is operable to measure the voltage, the circuit comprising:

a pass circuit having an input coupled between the internal node and a pin;

a reset circuit coupled to the pass circuit and operable to activate and reset the read circuit; and

a pass control circuit coupled to provide an output signal to the pass circuit that drives the pass circuit when active to pass the voltage at the node to the pin.

13. The circuit of claim 12, wherein the at least one circuit comprises a circuit that is operable to measure negative voltages.

14. The circuit of claim 12, wherein the at least one circuit comprises a circuit that is operable to measure high positive voltages.

15. The circuit of claim 12, wherein the at least one circuit comprises a circuit that is operable to measure negative voltages and a circuit that is operable to measure high positive voltages.

16. The circuit of claim 12, wherein the plurality of semiconductor devices comprises a dynamic random access memory.

17. The circuit of claim 12, wherein the at least one circuit comprises a pass gate coupled between the node and the pin such that the circuit passes a voltage from the node to the pin in a read mode and passes a voltage from the pin to the node in a force mode.

18. A method for controlling a semiconductor fabrication process, comprising the steps of:

fabricating a plurality of integrated circuits;

selecting at least one integrated circuit to test a voltage at an internal node;

measuring the internal voltage at a pin of the integrated circuit using a circuit fabricated on the same semiconductor substrate as part of the integrated circuit, the circuit comprising a pass circuit having an input coupled to the internal node and providing an output to the pin, a reset circuit coupled to the pass circuit and operable to activate and reset the read circuit, and a pass control circuit coupled to provide an output signal to the pass circuit that drives the pass circuit when active to pass the voltage at the node to the output pin; and

adjusting process parameters when an unacceptable voltage at the internal node is detected.

Abstract of the Disclosure

A circuit (10) for reading a voltage at a voltage source (14) of an integrated circuit (12). In one embodiment, the circuit (110) comprises a pass circuit (118) that has an input coupled to the node (114) of the integrated circuit (12). The circuit (110) provides a measurement of the voltage at the node (114) as an output to a pin (116). A reset circuit (122) is coupled to the pass circuit (118) and is operable to activate and reset the pass circuit (118). Finally, a pass control circuit (120) is coupled to provide an output signal to the pass circuit (118) that drives the pass circuit (118) when active to pass the voltage at the node (114) to the pin (116).

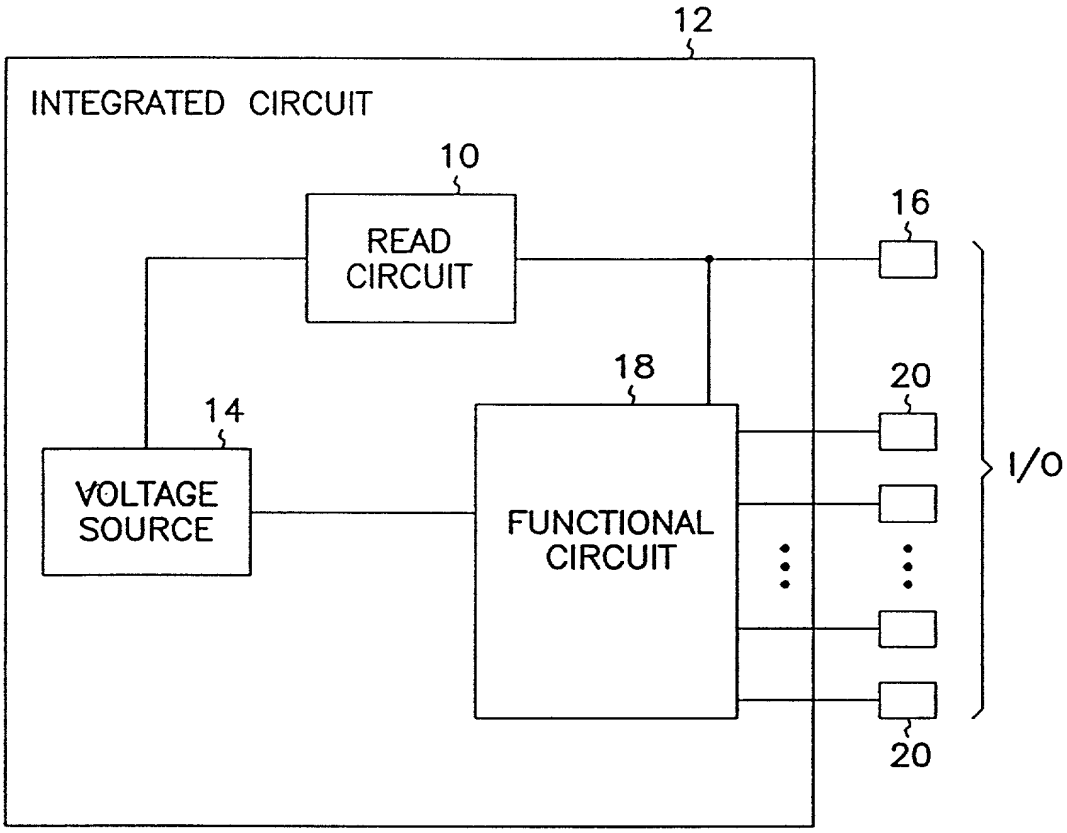

12
INTEGRATED CIRCUIT
10
READ CIRCUIT
16
18
20
14
VOLTAGE SOURCE
FUNCTIONAL CIRCUIT
I/O
20

FIG. 1

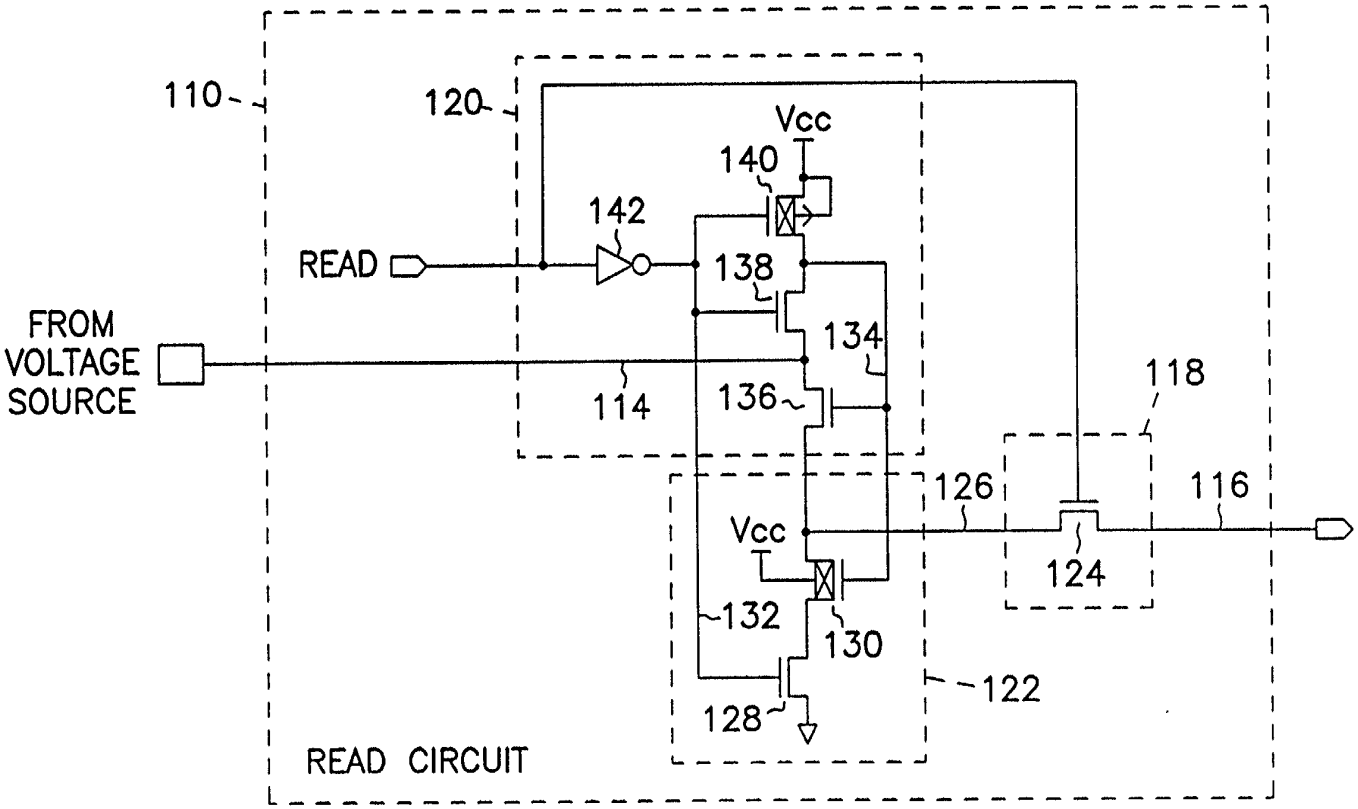


FIG. 2

FIG. 3A

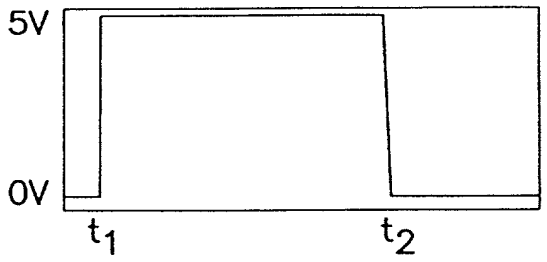


FIG. 3B

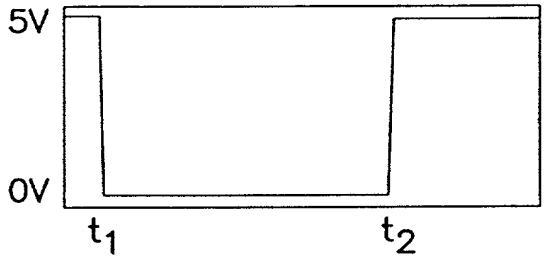


FIG. 3C

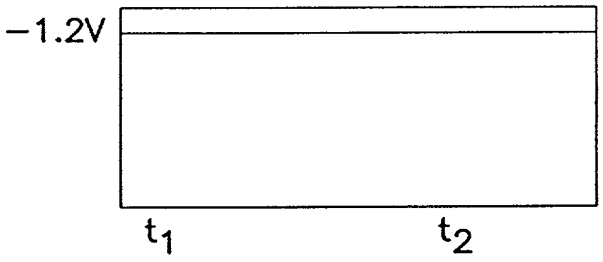


FIG. 3D

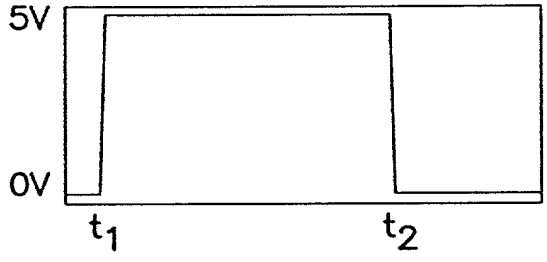


FIG. 3E

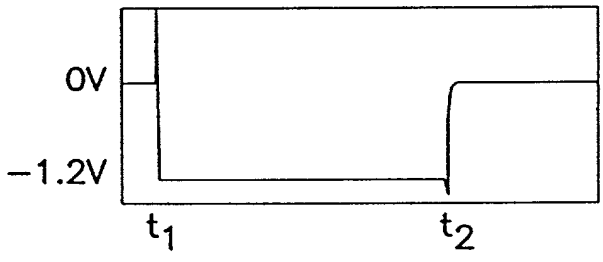
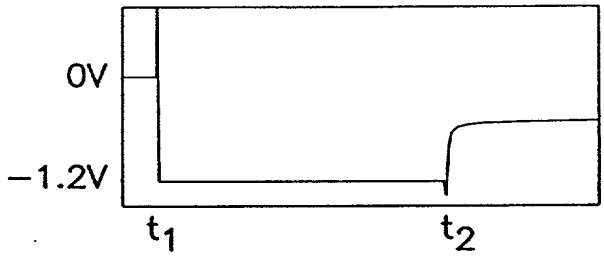


FIG. 3F



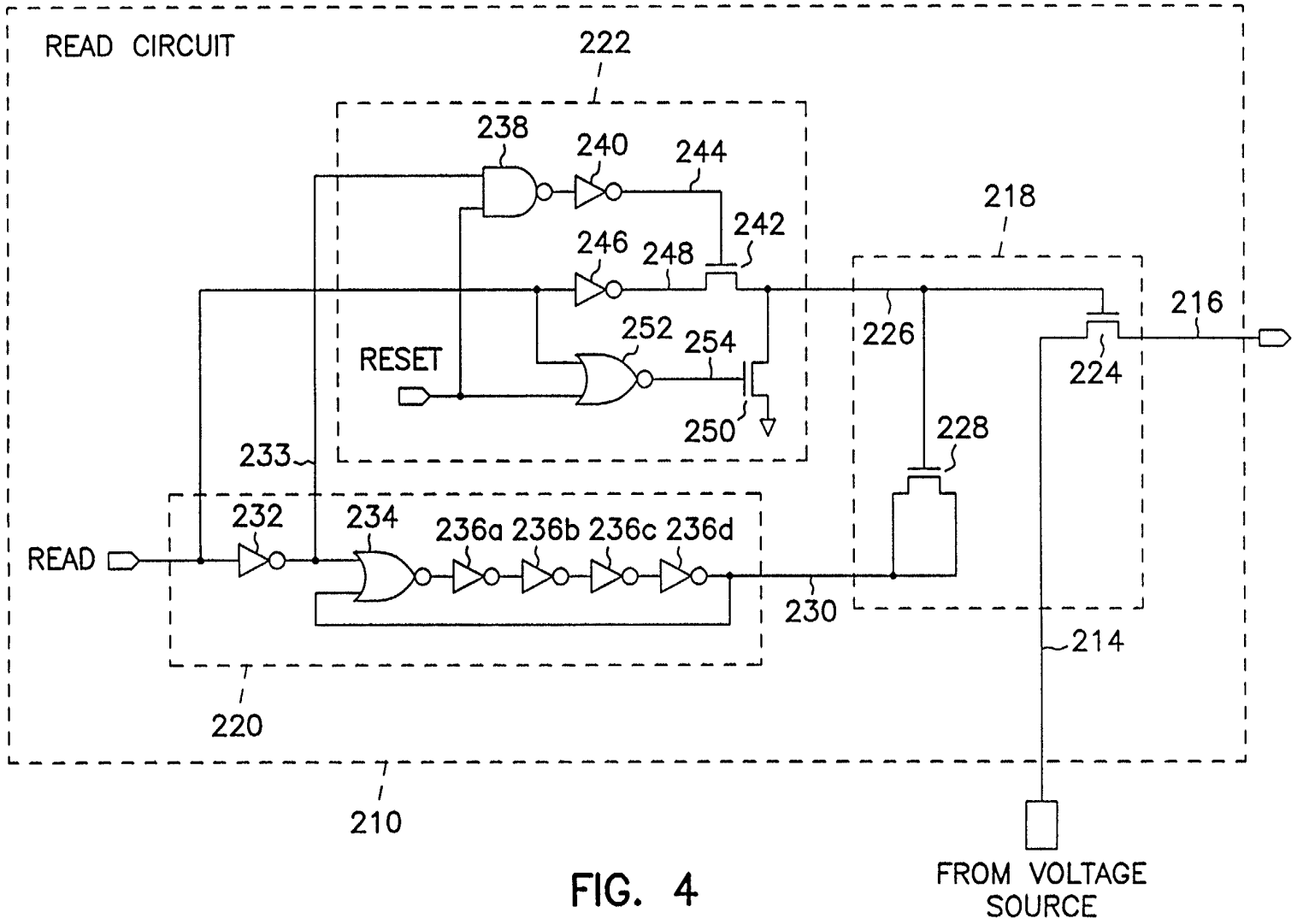

READ CIRCUIT
222
238
240
244
242
246
248
218
216
226
224
252
254
RESET
250
228
233
232
234
236a 236b 236c 236d
READ
230
214
220
210
FROM VOLTAGE SOURCE

FIG. 4

FIG. 5A

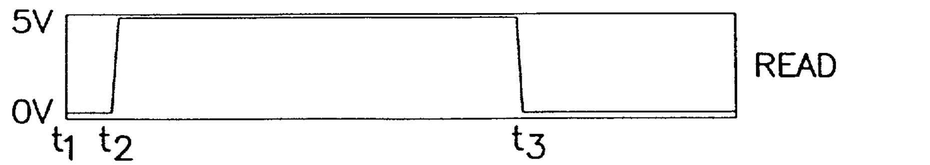


FIG. 5B

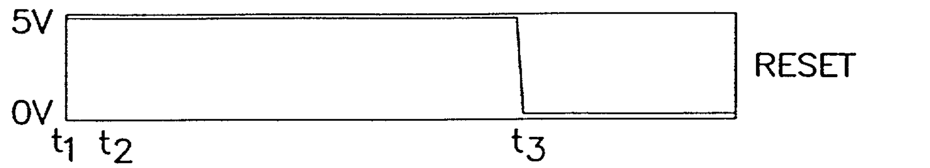


FIG. 5C

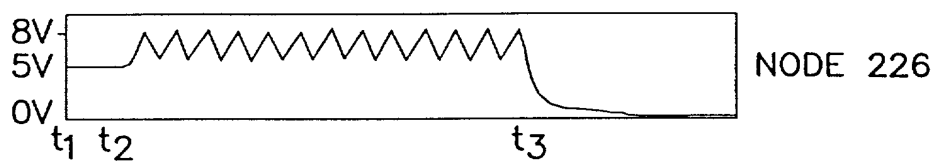


FIG. 5D

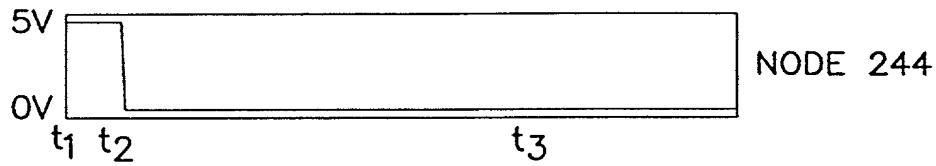


FIG. 5E

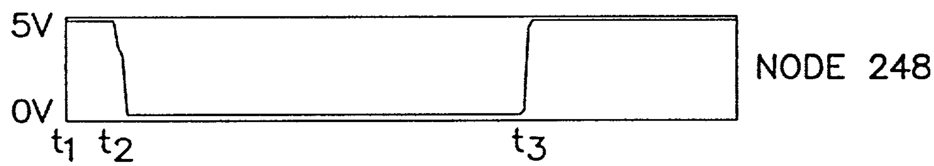


FIG. 5F

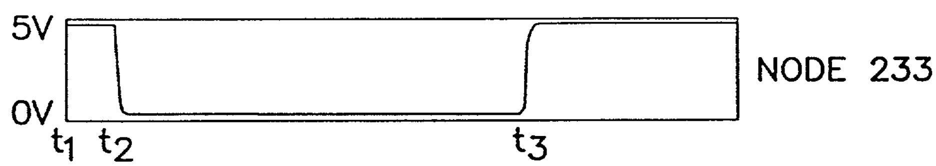


FIG. 5G

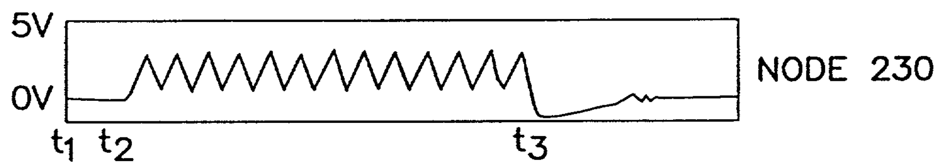


FIG. 5H

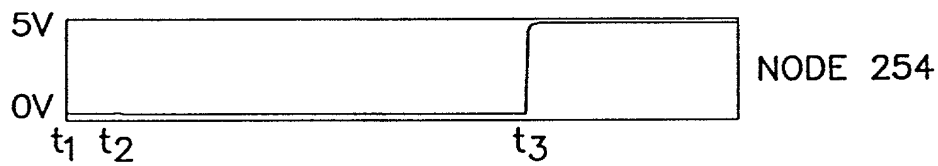


FIG. 5I

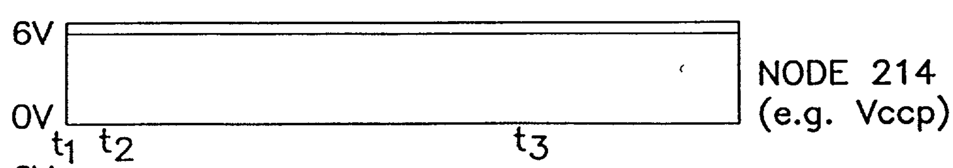
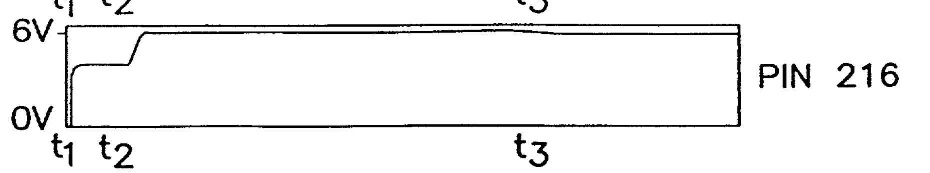


FIG. 5J



SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: CIRCUIT AND METHOD FOR MEASURING AND FORCING AN INTERNAL VOLTAGE OF AN INTEGRATED CIRCUIT .

The specification of which
a. X is attached hereto
b. ___ was filed on _____ as application serial no. _____ and was amended on _ (if applicable) (in the case of a PCT-filed application) described and claimed in international no. __ filed __ and as amended on _ (if any), which I have reviewed and for which I solicit a United States patent.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent of inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

a. X no such applications have been filed.
b. ___ such applications have been filed as follows:

FOREIGN APPLICATION(S), IF ANY, CLAIMING PRIORITY UNDER 35 USC § 119			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)

ALL FOREIGN APPLICATIONS, IF ANY, FILED BEFORE THE PRIORITY APPLICATION(S)			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in

the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

US APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS(patented, pending, abandoned)

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

Bianchi, Timothy E.	Reg. No P-39,610	Fogg, David N.	Reg. No. 35,138	Lundberg, Steven W.	Reg No. 30,568
Billig, Patrick	Reg No. 38,080	Forrest, Bradley A	Reg. No. 30,837	Lynch, Michael L.	Reg No. 30,871
Brennan, Thomas F	Reg No. 35,075	Forrest, Peter	Reg. No. 33,235	Schwegman, Micheal L	Reg. No. 25,816
Burke, John E.	Reg No. 35,836	Holloway, Sheryl S	Reg. No. 37,850	Slifer, Russell D.	Reg. No. P-39,838
Clark, Barbara J.	Reg No. 38,107	Kalinowski, Leonard J.	Reg. No. 24,207	Viksnins, Ann S.	Reg. No. 37,748
Dennison, Lia Pappas	Reg No 34,095	Kluth, Daniel J.	Reg. No. 32,146	Woessner, Warren D	Reg No. 30,440
Embretson, Janet E.	Reg. No. P-39,665	Lemaire, Charles A	Reg. No. 36,198		
Farney, W. Bryan	Reg No. 32,651	Lempia, Bryan J	Reg. No. P-39,746		

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/organization/who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Schwegman, Lundberg, Woessner & Kluth, P.A. to the contrary.

Please direct all correspondence in this case to Schwegman, Lundberg, Woessner & Kluth, P.A. at the address indicated below:
P.O. Box 2938, Minneapolis, MN 55402
Telephone No. (612)339-0331

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Daniel R. Loughmiller	Joseph C. Sher	Kevin G Duesman
Date 2-22-96	Date 2/22/96	Date 2-22-96

For Additional Inventors: __ Indicate here and attach sheet with same information, including date and signature.

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.